3V µP Supervisor Circuits

– Watchdog timer
– Brownout detection
– Power supply monitor

The IMP705R/S/T CMOS supervisor circuits monitor power-supply and battery voltage level, and µP/µC operation.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions. A reset is generated when the supply drops below 2.63V (IMP705R), 2.95V (IMP705S) or 3.08V (IMP705T). In addition, the IMP705 features a 1.6 second watchdog timer. The reset output is active LOW. A versatile power-fail circuit has a 1.25V threshold, useful in checking battery levels and other voltage levels. All devices have a manual reset ($\overline{MR}$) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in 8-pin DIP, SO and MicroSO packages.

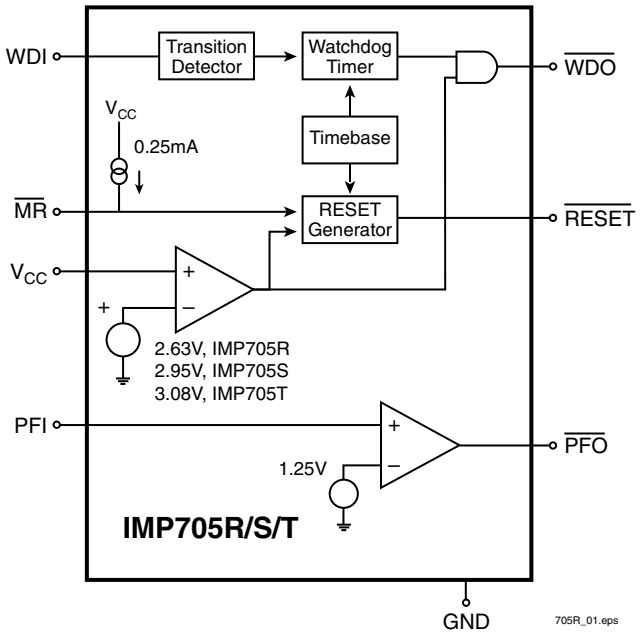
Key Features

- 140µA maximum supply current
- Three low voltage thresholds
  - 2.63V threshold (IMP705R)
  - 2.95V threshold (IMP706S)
  - 3.08V threshold (IMP706T)
- Debounced manual reset input
- Voltage monitor
  - 1.25V threshold
  - Battery monitor/Auxiliary supply monitor
- Watchdog timer
- 200ms reset pulse width
- Active LOW reset output
- DIP, SO and MicroSO packages

Applications

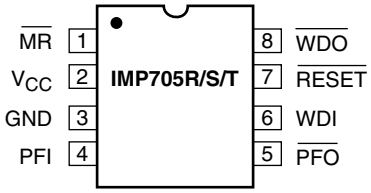
- Computers and embedded controllers
- Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

Block Diagrams

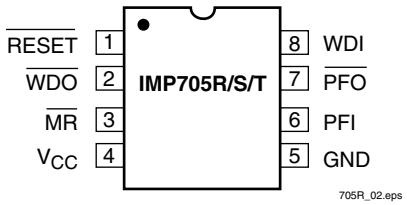


Pin Configuration

DIP/SO



MicroSO



Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
IMP705 Active LOW Reset, Watchdog Output and Manual RESET			
IMP705RCPA	2.63	0°C to +70°C	8-Plastic DIP
IMP705RCSA	2.63	0°C to +70°C	8-SO
IMP705RCUA	2.63	0°C to +70°C	8-MicroSO
IMP705RC/D	2.63	25°C	Dice
IMP705REPA	2.63	–40°C to +85°C	8-Plastic DIP
IMP705RESA	2.63	–40°C to +85°C	8-SO
IMP706SCPA	2.93	0°C to +70°C	8-Plastic DIP
IMP706SCSA	2.93	0°C to +70°C	8-SO
IMP706SCUA	2.93	0°C to +70°C	8-MicroSO
IMP706SC/D	2.93	25°C	Dice
IMP706SEPA	2.93	–40°C to +85°C	8-Plastic DIP
IMP706SESA	2.93	–40°C to +85°C	8-SO
IMP707TCPA	3.08	0°C to +70°C	8-Plastic DIP
IMP707TCSA	3.08	0°C to +70°C	8-SO
IMP707TCUA	3.08	0°C to +70°C	8-MicroSO
IMP707TC/D	3.08	25°C	Dice
IMP707TEPA	3.08	–40°C to +85°C	8-Plastic DIP
IMP707TESA	3.08	–40°C to +85°C	8-SO

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground

V_{CC} . . . . . −0.3V to 6.0V
All other inputs[1] . . . . . −0.3V to (V_{CC} + 0.3V)
Input Current at V_{CC} and GND 20mA
Output Current: All outputs 20mA
Rate of Rise at V_{CC} 100V/µs
Plastic DIP Power Dissipation . . . . . 700 mW
(Derate 9 mW/°C above 70°C)
SO Power Dissipation . . . . . 470 mW
(Derate 5.9 mW/°C above 70°C)
MicroSO Power Dissipation 330mW
(Derate 4.1 mW/°C above 70°C)

Operating Temperature Range

IMP705E . . . . . −40°C to 85°C
IMP705C . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 160°C
Lead Temperature Soldering(10 sec) . . . . . 300°C

Note: 1. The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

These are stress ratings only and functional operation is not implied.

Electrical Characteristics

Unless otherwise noted, V_{CC} = 4.75V to 5.5V and specifications apply over the operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage Range	V_{CC}		1.2		5.5	V
Supply Current	I_{CC}			75	140	µA
RESET Threshold	V_{RT}	IMP705R		2.63		V
		IMP705S		2.95		
		IMP705T		3.08		
RESET Threshold Hysteresis				40		mV
RESET Pulse Width	t_{RS}		140	200	280	ms
$\overline{MR}$ Pulse Width	t_{MR}		0.15			µs
$\overline{MR}$ to RESET Out Delay	t_{MD}				0.25	µs
$\overline{MR}$ Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
$\overline{MR}$ Pull-up Current		$\overline{MR}$ = 0V	100	250	600	µA
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		I_{SINK} = 3.2mA			0.4	
		V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
Watchdog Timeout Period	t_{WD}		1.00	1.60	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold	V_{IH}	V_{CC} = __V				V
	V_{IL}				0.8	
WDI Input Current		WDI = V_{CC}		50	150	µA
		WDI = 0V	−150	−50		
$\overline{WDO}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		I_{SINK} = 1.2mA			0.4	
PFI Input Threshold		V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current			−25	0.01	25	nA
$\overline{FPO}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		I_{SINK} = 3.2mA			0.4	

Pin Descriptions

Pin Number		Name	Function
DIP/SO	MicroSO		
1	3	$\overline{MR}$	Manual RESET input. The active LOW input triggers a reset pulse. A 250mA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	V_{CC}	+5V power supply input.
3	5	GND	Ground reference for all signals.
4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to ground or V_{CC} when not used.
5	7	PFO	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge.
7	1	$\overline{RESET}$	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold. $\overline{RESET}$ remains LOW for 200ms after V_{CC} rises above the $\overline{RESET}$ threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when V_{CC} is below the reset threshold, $\overline{WDO}$ remains low. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as V_{CC} exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
—	—	RESET	Active-HIGH reset output. RESET is the inverse of $\overline{RESET}$. The IMP813L has only a RESET output.

705R_t01.eps

Feature Summary

	IMP705R	IMP705S	IMP705T
Power-fail detector	■	■	■
Brownout detection	■	■	■
Manual RESET input	■	■	■
Power-up/down RESET	■	■	■
Watchdog timer	■	■	■
Active-HIGH RESET output			
Active-LOW RESET output	■	■	■
RESET threshold	2.63V	2.95V	3.08V

Detail Descriptions

$\overline{\text{RESET}}$ Operation

The $\overline{\text{RESET}}$ signal is designed to start a µP/µC in a known state or return the system to a known state.

$\overline{\text{RESET}}$ is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence, $\overline{\text{RESET}}$ remains low until the supply rises above the threshold level. $\overline{\text{RESET}}$ goes high approximately 200ms after crossing the threshold.

During power-down, $\overline{\text{RESET}}$ goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, $\overline{\text{RESET}}$ pulses low. If a brownout occurs during an already-initiated reset, the pulse will continue for a minimum of 140ms.

Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by a 250µA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

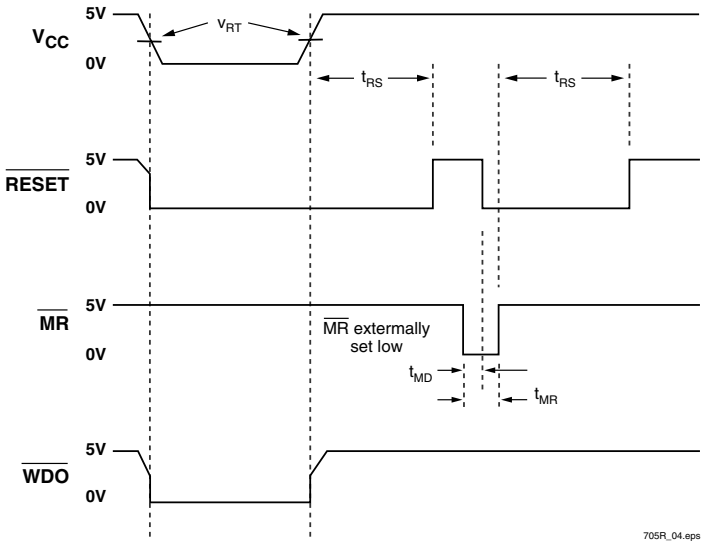
By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces $\overline{\text{RESET}}$ to be generated.

Watchdog Timer

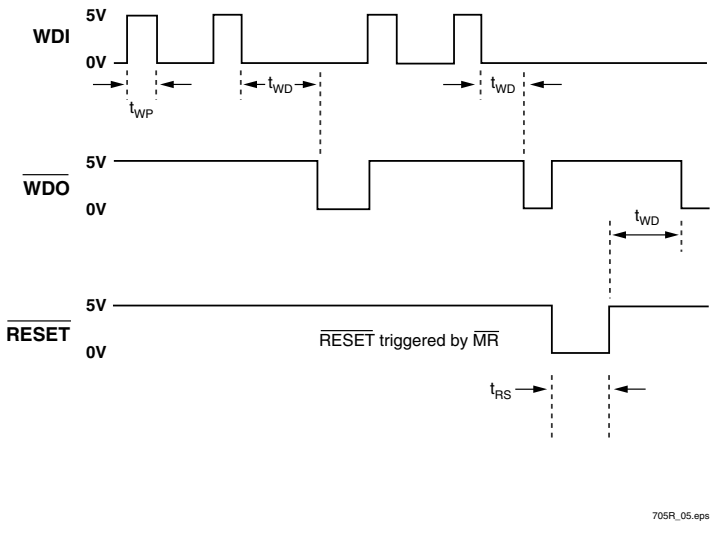
The watchdog timer monitors µP/µC activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{\text{WDO}}$ will also become LOW and remain so, whenever the supply voltage, V_{CC} , falls below the device threshold level. $\overline{\text{WDO}}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for $\overline{\text{WDO}}$ as there is for the RESET outputs. If WDI is floated, $\overline{\text{WDO}}$ essentially acts as a low-power output indicator.



WDI Three-state operation

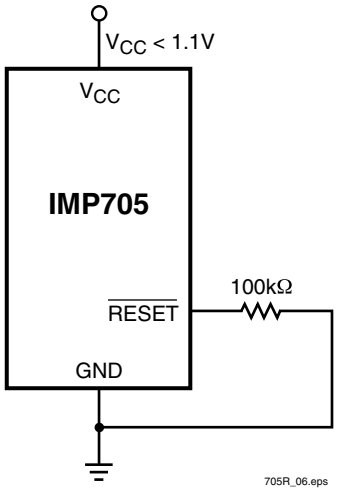


Watchdog Timing

Application Information

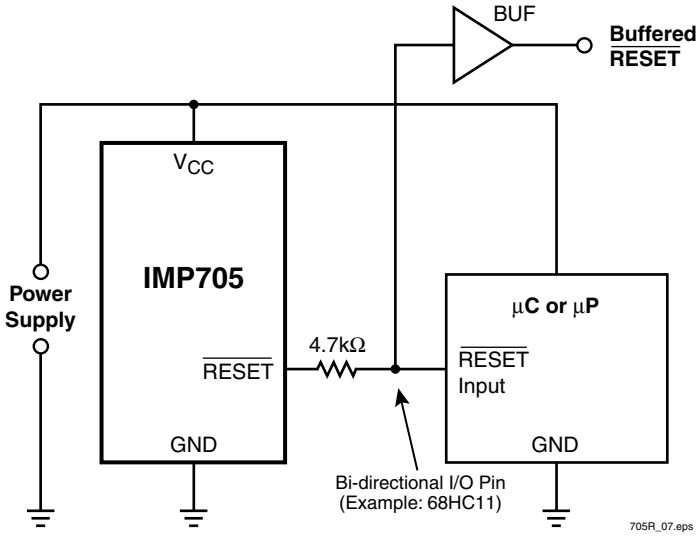
Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.1V, the IMP705 $\overline{\text{RESET}}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{\text{RESET}}$ to the wrong state, a pull-down resistor should be connected to the $\overline{\text{RESET}}$ in, thus draining such charges to ground and holding RESET low. The resistor value is not critical. A 100kΩ resistor will pull $\overline{\text{RESET}}$ to ground without loading it.

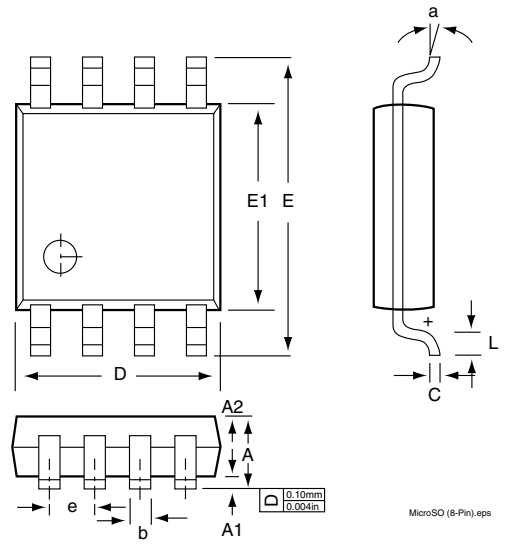


Bi-directional Reset Pin Interfacing

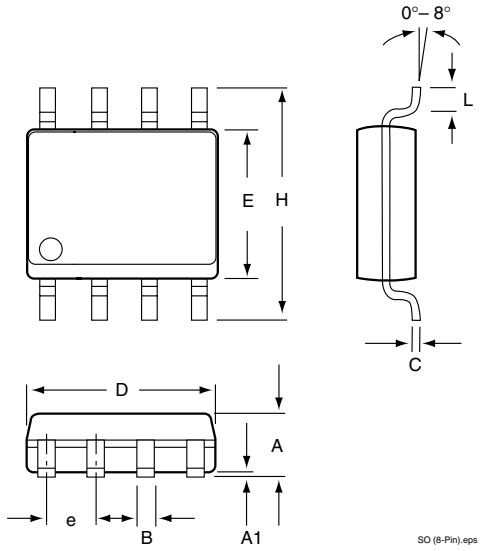
The IMP705 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the $\overline{\text{RESET}}$ output and the µP/µC bi-directional $\overline{\text{RESET}}$ pin.



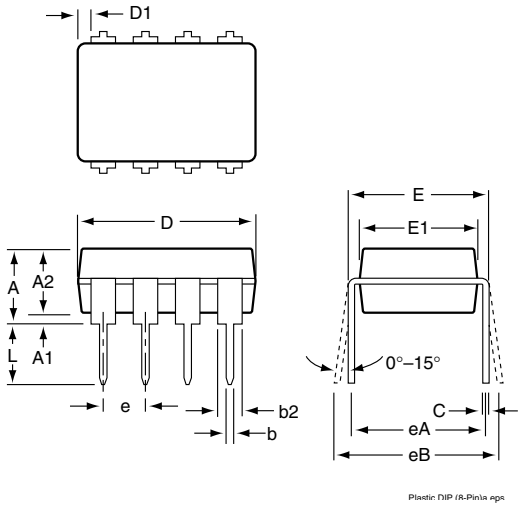
MicroSO (8-Pin)



SO (8-Pin)



Plastic DIP (8-Pin)



Package Dimensions

	Inches		Millimeters	
	Min	Max	Min	Max
MicroSO (8-Pin)*				
A	———	0.0433	———	1.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°
SO (8-Pin)**				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	2.00
Plastic DIP (8-Pin)***				
A	———	0.210	———	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81

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** JEDEC Drawing MO-187AA*
*** JEDEC Drawing MS-112AA*
**** JEDEC Drawing MS-001BA*

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IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134-2071
Tel: 408-432-9100
Tel: 800-438-3722
Fax: 408-434-0335
e-mail: info@impinc.com
http://www.impweb.com

Printed in USA
Publication #: 1021
Revision: A
Issue Date: 01/26/99
Type: Preliminary